Spintronics Work-Log

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Legend :

- Yellow Highlights → indicates a holiday, with the reason mentioned in parentheses.
- `problem` → this section talks about the problems faced that day.

`15 may` - came to Banaras
Internship starts

- `16 may` - hostel and other official formalities

- `17 may` - received research paper from Jagadish sir and started reading it (VK Joshi et al)

- `18 may` - off (Saturday)

- `19 may` - off (Sunday)

- `20 may` - finished reading and understanding the paper (VK Joshi et al), watched multiple videos to try and grasp the basics of spintronics

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- `21 may` - installed and started learning ngspice, learnt how to write basic netlists such as that of a Halfwave Rectifier.

- `22 may` - started learning about cmos logic , (inverter, Nand, nor and xor using cmos logic).

→ `problem` - all the other circuits - CMOS Inverter, CMOS NAND and CMOS NOR worked without any hiccups but the CMOS XOR design is giving incorrect output.

- `23 may` - off (Buddha Poornima)

- `24 may` - still worked on xor gate as it was not properly working on 22.

→ `problem` - XOR was not working earlier because inverters were incorrectly placed and the subcircuit for it had lot of issues, now the graph is 75% correct but the last test case still fails.

- `25 may` - off (Saturday)

- `26 may` - off (Sunday)

- `27 may` - xor implemented, made xor with Nand, sub circuital netlists, made half and full adder

→ `problem` - Solved some minor syntax issues in XOR netlist and it finally worked. There were also issues with the MOSFET model, which was fixed with help from Jagadish sir's model. Other circuits today, such as the XOR gate with NAND gates, Gate with subcircuits, Half adder with Nand subcircuits and Full-adder with Half adder subcircuits, were made without a lot of setbacks, with one or two tries.

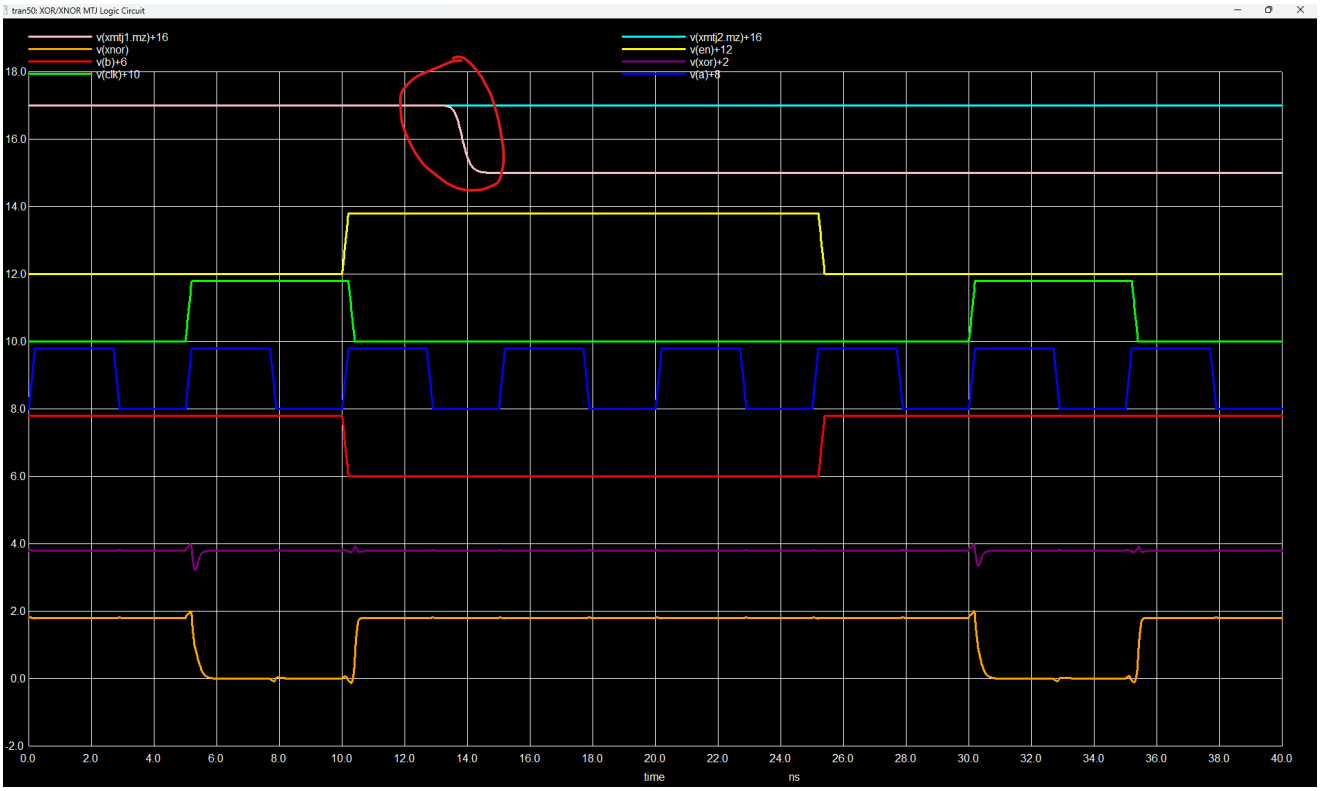
- `28 may` - received spice files to review and understand from Jagadish sir, simulated all of them separately and understood their outputs. Looked at information about the circuits which were new to me.

- `29 may` - tried to implement XOR XNOR Logic design with hybrid CMOS MTJ architecture.

→ `problem` - made the circuital netlist but could not write data into the MTJs, for the B signal to feed to the read transistors. redrew the diagram a couple of times to get the right circuit.

- `30 may` - still working on XNOR XOR logic with hybrid CMOS-MTJ architecture.

→ `problem` - figured out the right way to write data into MTJs but only one of them is getting switched. Also, both of them have the same initial magnetization as well as resistance which is odd, even tough the **th_in** parameter (initial theta) is 3.140 and 0.001 for the two MTJs (shown in the image below). tried many different combinations of W and L for the write drivers hoping the error was that it was not receiving enough current due to smaller than needed width, but the best result was still only one MTJ getting written.



Jagadish sir inspected the netlist and pointed out the missing "UIC" part in tran command. After that, and with some tweaks to the parameters of the mtj, the mtjs have different initial values and are switching accurately. But still, the reading transistor XOR and XNOR output is wrong.

- `31 may` - started the day with the same circuit from 30th may, by tweaking a few parameters in the "A" signal, got the correct result.
  Made all the other logic circuits present in the VK Joshi et al paper (NOR/OR and NAND/AND), with the right outputs, no setbacks faced.
  Read and tried to make sense of mtj cmos hybrid papers on IEEE Xplore dated post 2020. Searched and brainstormed ways to make optimal circuits which are preferably fully non-volatile, use minimal amount of write drivers, have good enough resistive difference for the PCSA to be able to sense easily, and the circuital operation takes minimum time.

- `1 june` - off (Saturday)

- `2 june` - off (Sunday)

- `3 june` - surfing on the internet, reading relevant recent papers and books and and trying to find ways to optimize circuits to make efficient cmos-mtj hybrid circuits. Developing concepts along the way as well.
  attended SCL 180nm PDK Webex meeting as directed by Ashok sir.
  Wrote netlist for and simulated the Separated Pre charge Sense Amplifier (SPCSA).

- `4 june` - brainstorming ways to make a way to make a reference point using different optimization techniques discovered in Erya Deng et al. - Design Optimization and Analysis of Multicontext STT-MTJ/CMOS Logic Circuits :
  1. transistor sizing variation
  2. dynamic mtj reference
  3. multi VT strategy (VT=threshold voltage)

- `5 june` - reading research papers and looking into articles talking about reconfigurable logic created using mtj. Read Reconfigurable logic for carry-out computing in 1-bit full adder using a single magnetic tunnel junction by Gi Yoon Bae et al. and Full adder based Reconfigurable Spintronic ALU using STT-MTJ by Lokesh B. et al. thoroughly.

Working on making a hybrid imtj and ipmtj model by combining the University of Minnesota MTJ Models, which will help optimize circuits tremendously.

- `6 june` - Continuing work on trying to make a SPICE model for a hybrid ipmtj and imtj MTJ model. Figuring out how to properly account for the additional barrier layer and common free layer. Made a basic model and now trying to implement it in HSPICE using Mobaxterm remote access.

- `7 june` - There seem to be a lot of logic errors in the netlist due to the conflicting 'thi' parameter in the LLG solver which is significantly different for both the types of RL. Simulating the model using MTJ_write.sp file in hspice like yesterday and fixing the errors along the way.

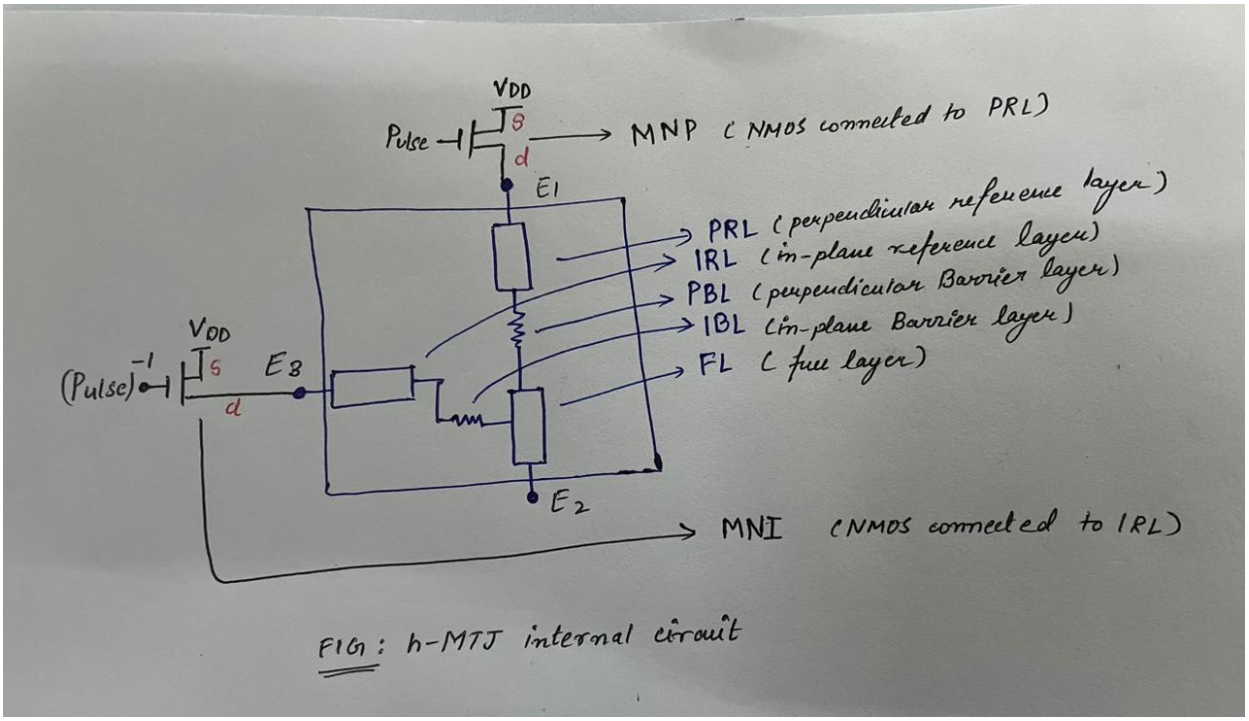
  → `problem` - the model is working on Hspice if we don't include the secondary electrode ve2 along side the original electrode ve1, which if done gives the error: Inductor/voltage source loop found containing 1:ve2 defined in subckt mtj. Apart from this, the wave-view plot viewer is not working with mobaxterm even tough the X server is on and X11 forwarding is active.

- `8 june` - off (Saturday)

- `9 june` - off (Sunday)

- `10 june` - Still working on the model. Tried plotting the graph on hspice wave view on the main computer on 7th June, which did run, but the graph is not correct at all. Solved the secondary electrode issue by introducing a separate common node "ex2", but the graph is still straight and no switching or activity is visible, so working towards that. removed type parameter and replaced it with "MA" instead as to reduce redundancy in

parameters.



- `11 june` - adding two 2 nmos transistors with opposite pulses at the 2 RLs in order to make sure that both of them do not have potential simultaneously. the graphs are no longer straight lines and some activity is seen but successful switching of mtj does not seem to happen.

- `12 june` -

- `13 june` -

- `14 june` -

- `15 june` - off (Saturday)

- `16 june` - off (Sunday)

Internship Ends

Fig: XOR Correct circuit from 29th May